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High Frequency RF Source for High Data Rate Modulation Techniques

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Abstract— there are various modulation schemes that are used in communication system. The modulating signal and the carrier play an important role. There are different methods to build (Numerically Controlled Oscillator) NCOs like Look-Up Table (LUT), Cordic algorithm, Xilinx built-in BRAM (Block RAM) and Slices. This paper presents Xilinx BRAM based method of generating high speed, high frequency sine and cosine digitally synthesized RF wave. The proposed method could generate high frequency signal with nearly 45% faster locking time with respect to Look-Up Table (LUT) based NCO and 60% faster locking time with respect to Cordic based NCO.

Keywords: NCO-Numerically Controlled Oscillator, LUT-Look up Table, DAC-Digital to Analog Converter. SFDR- Spurious Free Dynamic Range, DDS-Direct Digital Synthesizer, BRAM- Block Random Access Memory, PLL-Phase Locked Loop

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1. INTRODUCTION

A NCO is a digital signal generator which creates a synchronous (i.e. clocked), discrete-time, discrete-valued representation of a waveform, usually sinusoidal. NCOs are often used in conjunction with a digital-to-analog converter (DAC) at the output to create a direct digital synthesizer (DDS) [1].

Numerically controlled oscillators offer several advantages over other types of oscillators in terms of agility, accuracy, stability and reliability. NCOs are used in many communication systems including digital up/down converters used in 3G wireless and software radio systems, digital PLLs, radar systems, drivers for optical or acoustic transmissions, and multilevel FSK/PSK /QAM modulators /demodulators. Figure 1 shows the general block diagram of communication system.

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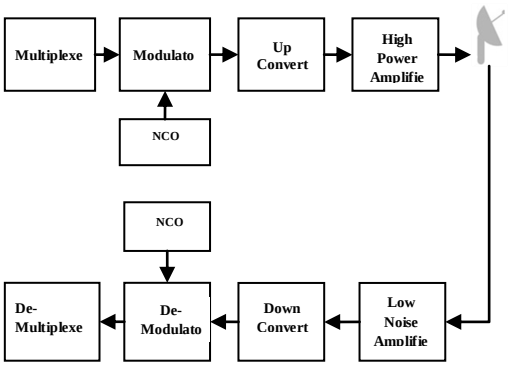


Figure 1: Communication System Block Diagram

In the communication system the modulator at transmitter side and demodulator at the receiver side requires RF source, which is obtained through NCO.

The most common techniques for implementing an NCO are [4],

- LUT based NCO
- CORDIC algorithm based NCO
- Xilinx BRAM based NCO

The LUT based NCO, the LUT is used to generate the data feed back signal. In this technique the ROM is used to store the samples of the sinusoid which are then read out at appropriate time intervals to produce the sinusoidal signal.

The addresses of the ROM are pointed by the LUT pointer and there is no auto increment of the address [2].

A second method for implementing an NCO is based upon the use of the Cordic Algorithm. This approach is similar to the ROM table-look-up approach except that the samples of the sinusoid are generated by an iterative algorithm rather than being stored in a ROM [3].

In Xilinx BRAM based technique the core is used to store the samples of the sinusoid which are then read out at appropriate time intervals to produce the sinusoidal signal. It consists of two parts: counter implemented by slices and sine/cosine lookup table implemented by Xilinx ROM (BRAM or distributed memory). Counter is an automated address generator and does not require any pointer to point the memory. Improvement in the frequency resolution can be achieved using trigonometric interpolation [4].

2. Design of Xilinx BRAM based NCO

Very high performance is achieved with optimal and optional use of DSP48 slices.

- Sine, Cosine, or quadrature outputs can be generated.
- Look-up table can be allocated to distributed or block memory.
- Phase dithering or Taylor series correction options provide high dynamic range signals using minimal FPGA resources.
- SFDR range is 18 dB to 120 dB.
- Phase dithering removes the spectral line structure associated with conventional phase truncation waveform synthesis architectures
- High-precision synthesizer with fine frequency resolution (Δf = 0.11Hz @ f_{clk} = 500 MHz, 32-bit phase accumulator) can be obtained.

The output frequency f_{out}, of the waveform is a function of the system clock frequency f_{clk}, the number of bits n in the phase accumulator and the phase increment value $\Delta\theta$. That is,

$$f_{out} = \Delta\theta f_{clk} / 2^n \ldots\ldots\ldots (1)$$

The frequency resolution Δf of the synthesizer is a function of the clock frequency and the number of bits employed in the phase accumulator. That is,

$$\Delta f = f_{clk}/2^n \ldots\ldots\ldots\ldots (2)$$

3. Implementation

The implementation of Xilinx BAM based NCO is done in VHDL and the values are plotted in MATLAB is as shown in figure 2. It consists of a phase accumulator and a phase-to amplitude converter (PAC). The components A1 (adder) and B1 (register) computes phase slope that is mapped to a sinusoid by PAC.

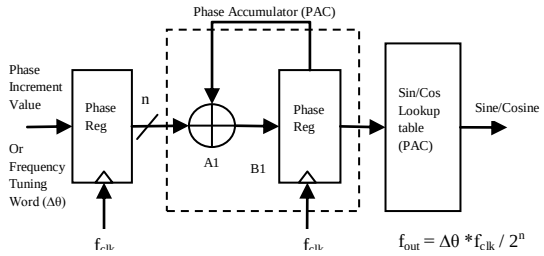


Figure 2: Block diagram of NCO

Operation:

3.1. Phase Accumulator: The PA is a counter, which increments each time it receives a clock pulse. The magnitude of the increment is determined by the frequency tuning word and it effectively sets how many points to skip around the phase wheel and this word forms the phase step size between reference-clock updates. The larger the jump size, the faster the phase accumulator overflows and completes one full round of the phase wheel [5].

3.2. Sine/Cosine ROM: This is phase to amplitude converter which converts digital phase input from the accumulator to output amplitude. This output represents the phase of the wave as well as an address to a word, which is the corresponding amplitude of the phase in the ROM. After each clock cycle,

the appropriate magnitude of the ROM output is assigned to create a complete sine wave. The range of NCO is Fmin= Fclk/2*n, Fmax=Fclk/2. For Fclk=500 MHz, the range is 0.116 Hz to 250 MHz.

4. Simulation results:

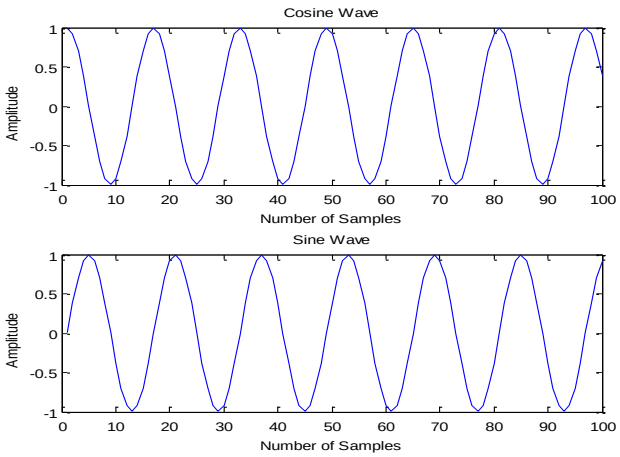
The results of VHDL program are written to a file and plotted in MATLAB

4.1. Example 1

Clock frequency, f_{clk}= 500MHz,

Number of bits of accumulator, n= 32

Outpot frequency, f_{out}=31.25MHz

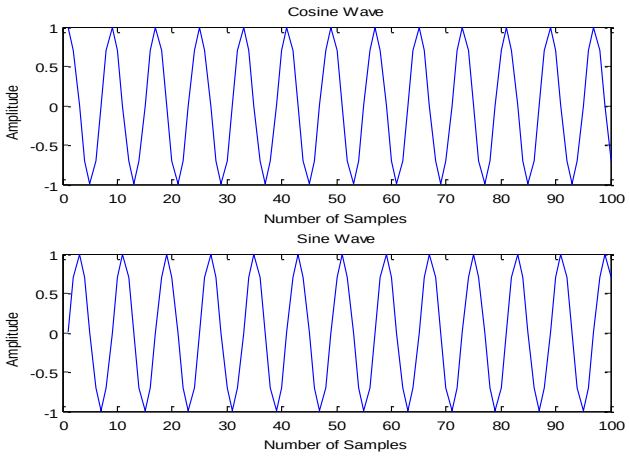


4.2. Example 2

Clock frequency, f_{clk}= 500MHz,

Number of bits of accumulator, n= 32

Output frequency, f_{out}=62.5MHz

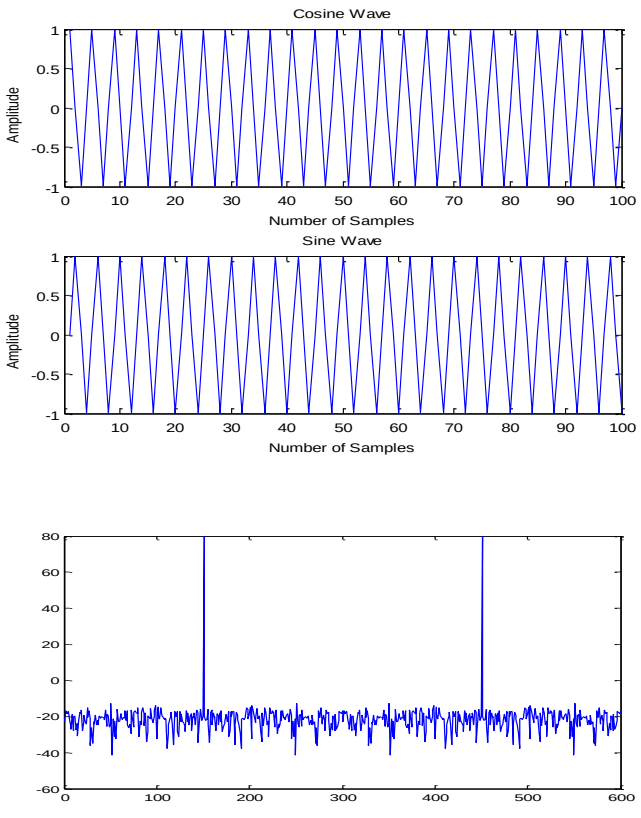


4.3. Example 3

Clock frequency, f_{clk}= 500MHz,

Number of bits of accumulator, n= 32

Output frequency, f_{out}=125MHz



SFDR = -96db

5. Conclusion

Table I: Synthesis Report of different NCO techniques [4].

	LUT based NCO	**CORDIC based NCO**	**Xilinx BRAM based NCO**
4-Input LUT	411	275	300
Slices	239	152	164
Gate Count	4113	3194	3228

Table II: Summarized Analysis of Different NCO techniques [4].

	LUT based NCO	**CORDIC based NCO**	**Xilinx BRAM based NCO**
Locking Time	11.73 us	16.975 us	6.315 us
Phase Angle	53 deg.	21 deg.	19 deg.
Tracking Range	~75MHz	~64 MHz	~75 MHz

From Table 1, it is easily visible that synthesis wise NCO using CORDIC occupied less area. But simulation proved that NCO using Xilinx ROM provided a faster locking time and better tracking frequency range.

Table 2 shows, the Xilinx ROM implementation of the NCOs has the lowest locking time, followed by the LUT based NCO, then the CORDIC NCO. If the area is not an issue the Xilinx core NCO is the best choice.

Hence the Xilinx BRAM based NCO generate high speed signal with nearly 45% faster locking time with respect to LUT based NCO and 60% faster locking time with respect to Cordic based NCO .

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